ABSTRACT OF THE DISCLOSURE

When power stoppage of a main power supply is detected during a normal operation, a power controller switches a power supply for a DRAM from the main power supply to a battery power supply and makes an instruction signal for instruction a self-refresh mode to a memory controller active. In response to this, the memory controller changes a clock enable signal for the DRAM to a low level to establish the self-refresh mode of the DRAM, and, after, the self-refresh mode of the DRAM is established, supplying of power to the memory controller is stopped. The clock enable signal for the DRAM is maintained to the low level by pull-down resistance even when the supplying of power to the memory controller is stopped from a condition that the signal is changed to the low level in the self-refresh mode, thereby maintaining the self-refresh mode of the DRAM.